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Micron Technology, Inc.
c/o Tom D'Amico
Dickstein, Shapiro, Moran & Oshinsky
2101 L Street, NW
Washington, DC 20037-1526

EXAMINER	
LONG, HEATHER R	

ART UNIT	PAPER NUMBER
2615	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,785	KRYMSKI, ALEXANDER I.	
	Examiner	Art Unit	
	Heather R Long	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Page 4, line 5: reference sign "100".

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Fig. 1, reference sign "102" and "CB".

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borg et al. (U.S. Patent 6,476,864) in view of Fossum et al. (U.S. Patent 5,949,483).

Regarding claim **1**, Borg et al. discloses in Figs. 3B and 7 a signal chain for an image sensor, comprising: a plurality of photo sensing elements (10); a plurality of pixel readout circuits, wherein the output of the pixel readout circuit will be measure with respect to a reference signal (88); and an amplifier (230) configured to receive the reference signal (88), and to supply the reference signal to the plurality of pixel readout circuits during computation of the difference signal, where the amplifier (230) amplifies the difference signal when the computation is completed (col. 6, lines 39-43; col. 6, line 61 – col. 7, line 3). However, Borg et al. fails to disclose the details of the pixel readout circuits. Therefore, Borg et al. does not teach that each pixel readout circuit operates to receive a charge-induced signal and a reset signal from a photo sensing element, in order to compute a difference signal between the charge-induced signal and the reset signal, the difference signal being measured with respect to the a reference signal.

Referring to the Fossum et al. reference, Fossum et al. discloses in Fig. 3A a signal chain for an image sensor, comprising: a plurality of photo sensing elements (10); and a plurality of pixel readout circuits (70), each pixel readout circuit (70) operating to receive a charge-induced signal and a reset signal from a photo sensing element (10), and to compute a difference signal between the charge-induced signal and the reset signal (col. 6, line 54 – col. 7, line 27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Fossum et

al. with Borg et al. in order to obtain an output signal from the pixel readout that minimizes the effects of kTC noise.

Regarding claim **2**, Borg et al. discloses in Fig. 3B a signal chain, further comprising: a plurality of A-to-D converters operating to alternately convert the amplified difference signal (col. 6, line 61 – col. 7, line 3).

Regarding claim **6**, Fossum et al. discloses in Fig. 3B a signal chain, further comprising: a multiplexer configured to sequentially output saved difference signals (col. 9, line 59 – col. 10, line 11). Fossum et al. does not teach that the multiplexer outputs saved in the latch. However, this would be obvious if the multiplexer was positioned at the output of an A-to-D converter since most converters contain latches. Furthermore, Borg et al. teaches placing a multiplexer after an A-to-D converter (col. 6, line 66 – col. 7, line 3).

Regarding claim **7**, Borg et al. discloses in Fig. 3B a signal chain, wherein the plurality of photo sensing elements (10) is a pixel array in columns of pixels.

Regarding claim **8**, Fossum et al. discloses in Fig. 3A a signal chain, wherein each pixel readout circuit (70) includes at least two capacitive elements (CS, CR, and 116), one to hold pixel reset value (CR), and another to compute and store the difference signal between the charge-induced signal and the reset signal (116) (col. 6, line 54 – col. 7, line 27).

Regarding claim **9**, Borg et al. discloses a signal chain, wherein the amplifier includes a feedback switch operating to provide the reference signal,

received at a negative input to the amplifier, to each pixel readout circuit through a feedback (col. 10, lines 61-65).

Regarding claim **10**, Fossum et al. discloses a signal chain, wherein each pixel readout circuit includes a column select switch (220) to connect selected column pixel readout to the amplifier (col. 6, line 60-63).

Regarding claim **11**, Fossum et al. discloses a signal chain, wherein the column select switch (220) is a MOSFET transistor (col. 6, lines 60-63). However, Fossum et al. fails to teach that the MOSFET is a p-channel MOSFET. Official Notice is taken that both the concept and the advantages of a p-channel MOSFET are both well known and expected in the art.

Regarding claim **12**, Fossum et al. discloses a signal chain, wherein each pixel readout circuit includes a sample and hold switch (116) to sequentially read the charge-induced signal and the reset signal.

Regarding claim **13**, Fossum et al. discloses a signal chain, wherein the sample and hold switch (116) is a MOSFET transistor (col. 6, line 54 – col. 7, line 27). However, Fossum et al. fails to teach that the MOSFET is an n-channel MOSFET. Official Notice is taken that both the concept and the advantages of an n-channel MOSFET are both well known and expected in the art.

Regarding claim **14**, Borg et al. discloses in Fig. 7 a signal chain, further comprising: a sample and hold circuit (142) coupled to the reference signal, the sample and hold circuit operating to provide a stable reference signal (col. 11, lines 15-17).

Regarding claim **15**, Borg et al. discloses in Fig. 5 a signal chain, wherein the signal smoothing circuit includes: a reference signal generator (88) operating to generate the reference signal (88); at least one switch (84) configured to sample and hold the reference signal (88) at a certain level; and a capacitor (82) coupled to at least one switch, the capacitor (82) operating to hold the sampled value at the certain level (col. 8, lines 64-66).

Regarding claim **16**, Borg et al. in view of Fossum et al. differs from claim 16 in that claim 16 further requires the reference voltage generator to include a voltage divider resistor network. However, Official Notice is taken that both the concept and the advantages of using a voltage divider resistor network to provide a reference voltage generator is well known and expected in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a voltage divider resistor network as a reference voltage generator because the resistor voltage divider is used to supply a voltage different from that of an available battery or power supply.

Regarding claim **17**, Borg et al. fails to disclose in Fig. 5 that the switch (84) includes a MOSFET transistor. However, official notice is taken that both the concept and advantages of using a MOSFET transistor is well known and expected in the art. Therefore, it would have been obvious to use a MOSFET transistor for the switch (84) as disclosed by Borg et al.

Regarding claim **18**, Borg et al. discloses an image sensor output circuit, comprising: a pixel array (280) having a series of pixels, and operating to receive

optical data and convert the optical data into electrical signals; readout circuits that will later compare their outputs with a reference signal (88); an amplifier (230) configured to provide the reference signal (88) while the readout circuit is reading the electrical signal, and to provide amplification of the referenced electrical signals when the reading is done; and at least one A-to-D converter (220) operating to provide conversion of the amplified electrical signal (col. 6, lines 39-43; col. 6, line 61 – col. 7, line 3). However, Borg et al. fails to disclose the details of the pixel readout circuits.

Referring to the Fossum et al. reference, Fossum et al. discloses an image sensor output circuit, comprising: a pixel array; and readout circuits (70) configured to read the electrical signals from the series of pixels (10) (col. 6, line 54 – col. 7, line 27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Fossum et al. with Borg et al. in order to provide a readout circuit that reads the electrical signals from the signals and compares them to a reference signal to eliminate noise components.

Regarding claim **19**, Borg et al. discloses in Fig. 3B an image sensor output circuit, wherein at least one A-to-D converter (220) includes first and second A-to-D converters (220), the first A-to-D converter converting the reference electrical signal while the second A-to-D converter is sampling a next reference electrical signal (col. 6, line 66 – col. 7, line 3).

Regarding claim **20**, Fossum et al. discloses in Fig. 3B an image sensor output circuit, further comprising: a multiplexer configured to sequentially output converted signals (col. 9, line 59 – col. 10, line 11).

Regarding claim **21**, Borg et al. discloses an image sensor comprising: a pixel array (280) having a plurality of pixels (10); a plurality of pixel readout circuits, wherein the output of the pixel readout circuit will be measure with respect to a reference signal (88); an amplifier (230) coupled to each pixel readout circuit, the amplifier (230) configured to supply the reference signal (88) during computation of the difference signal, and to amplify the difference signal when the computation is done; a pixel array addressing circuit (210) configured to select a group of pixels in the pixel array (280) to readout; and a controller (200) coupled to the pixel array addressing circuit (210), and operating to provide selection control to the pixel array addressing circuit (210) (col. 6, lines 39-43; col. 6, line 61 – col. 7, line 3). However, Borg et al. fails to disclose the details of the pixel readout circuits. Therefore, Borg et al. does not teach that each pixel readout circuit operates to receive a charge-induced signal and a reset signal from a pixel of the pixel array, and to compute a difference signal between the charge-induced signal and the reset signal, the difference signal being measured with respect to a reference signal.

Referring to the Fossum et al. reference, Fossum et al. discloses in Fig. 3A an image sensor, comprising: a pixel array having a plurality of pixels (10); and a plurality of pixel readout circuits (70), each pixel readout circuit (70)

operating to receive a charge-induced signal and a reset signal from a pixel (10) of the pixel array, and to compute a difference signal between the charge-induced signal and the reset signal (col. 6, line 54 – col. 7, line 27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Fossum et al. with Borg et al. in order to obtain an output signal from the pixel readout that minimizes the effects of kTC noise.

6. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borg et al. in view of Fossum et al. as applied to claims 1 and 2 above, and further in view of Pezzini et al. (U.S. Patent 6,124,821).

Regarding claim **3**, Borg et al. in view of Fossum et al. differs from claim 3 in that claim 3 further requires the signal chain, wherein each of the plurality of A-to-D converters include a binary-scaled capacitor network capable of sampling and converting the reference signal to a digital value.

Referring to the Pezzini et al. reference, Pezzini et al. discloses a binary-scaled capacitor network for an A-to-D converter capable of sampling and converting the reference signal to a digital value (col. 2, lines 23-37; and col. 4, lines 36-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Pezzini et al. with Borg et al. in view of Fossum et al. in order to provide an analog-to-digital

converter that would convert an analog signal to a digital signal using binary code.

Regarding claim **4**, Borg et al. differs from claim 4 in that claim 4 further requires the plurality of A-to-D converters to include a latch to save the converted difference signal. However, Borg et al. discloses a plurality of A-to-D converters in Fig. 3B, but does not show the details of them. Official Notice is taken that both the concept and the advantages of the A-to-D converters including a latch to save the converted difference signal are well known and expected in the art. Furthermore, this concept would have been obvious because most A-to-D converters comprise a comparator, which often include latches built inside them.

Regarding claim **5**, Borg et al. discloses in Fig. 3B a signal chain, wherein the plurality of A-to-D converters (220) include: a first A-to-D converter arranged into a first configuration operating to convert the amplified difference signal in a particular cycle; and a second A-to-D converter arranged into a second configuration operating to sample a next amplified difference signal into the binary scaled capacitor network (as disclosed by Pezzini et al.) in the particular cycle, wherein the first and the second A-to-D converters switch configurations in a cycle after the particular cycle (col. 6, line 61 – col. 7, line 3).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Cotter et al. (U.S. Patent 5,852,415) discloses an A-to-D converter with a binary-scaled capacitor network.

b. Chou (U.S. Patent 6,201,572) discloses a readout circuit for an active pixel sensor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather R Long whose telephone number is 703-305-0681. The examiner can normally be reached on Mon. - Thurs.: 7:00 am - 4:30 pm, and every other Fri.: 7:00 am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HRL
March 22, 2004

NGOC-YEN VU
PRIMARY EXAMINER